GT-17-265

Signal Integrity Characterization Report

Ochito “Blue” Contacts and Cable Assemblies for USB3.1 Gen 1 Application

P/N: 83H-85179 – PCB-Mount Pin Contact
P/N: 83H-85178 – PCB-Mount Socket Contact
P/N: 858-028-02 – Cable Crimp Socket Contact
P/N: 858-029-02 – Cable Crimp Pin Contact
P/N: 792-009-10 – PCB-Mount R/A Pin Contact
P/N: 8572-0002-02-12 – 0.3m Cable Assembly
P/N: 8572-0002-02-59 – 1.5m Cable Assembly
P/N: 8572-0002-02-71 – 1.8m Cable Assembly

Revision History

Rev	DCN #:	Date	Issued By:	Approved By:
1	N/A	12/27/2017	Chansy Phommachanh	Guido Hunziker
2	N/A	9/7/2018	Chansy Phommachanh	Guido Hunziker

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Scope

The primary goal of this document is to qualify the high-speed signal integrity (SI) performance of the Glenair 8-position Ochito “Blue” contacts and cable assemblies intended for use in the USB 3.1 Gen 1 data protocol application. The contacts under qualification test include the PCB-mount, the cable crimp, and the right angle versions.
This document also covers the Ochito “Blue” cable assembly construction as USB connectivity components and the test methods of the cable assemblies and of the mated contact by itself. The Ochito cable assemblies were built using the components listed in this document and tested for SI performance parameters and specification defined in the USB 3.1 standard.

Application

In USB 3.1 application, a 4-pair 90-Ohm cabling system is required to support the data transmission at 5Gbps and higher. For the Ochito “Blue” contact, two differential pairs opposite side of one another are assigned and designated to carry the high-speed data transmission. The two pairs which are directly opposite from each other provide a distance for a superior crosstalk performance and less interference from the transmitting pair to the receiving pair. Third pair designated as “D+/D-“ lane is assigned to support the bi-directional USB 2.0 transmission at 480Mbps data rate for backward-compatible with the USB 2.0 connectivity solution. The fourth pair carries a power supply from the host to an USB device.

Reference Industry Standards

- USB 3.1 Connectors and Cable Assemblies Compliance Documents, July 2013.
- USB 2.0 Cables and Connectors Class Documents, April 2000.

Test Samples

The following Glenair Ochito “Blue” contact, bulk cable, and cable assembly part numbers were used for the SI sample test:

- P/N: 858-028-02 – Ochito Crimp Socket contact Assembly
- P/N: 858-029-02 – Ochito Crimp Pin Contact Assembly
- P/N: 792-009-10 – Ochito PCB-Mount Right Angle Contact Assembly for Test Fixture
- P/N: 83H-85178 – Ochito PCB-Mount Socket Contact Assembly for Test Fixture
- P/N: 82H-85179 – Ochito PCB-Mount Pin Contact Assembly for Test Fixture
- P/N: 963-110 – USB 3.0 Bulk Cable
- P/N: 8572-0002-02-59 – 1.5m Pin to Socket Ochito “Blue” Cable Assembly
- P/N: 8572-0002-02-12 – 0.3m Pin to Socket Ochito “Blue” Cable Assembly
- P/N: 8572-0002-02-71 – 1.8m (0.3m + 1.5m Lengths) Cable Assembly

Ochito “Blue” Contact Pin/Pair Assignment

Pin and pair assignments of the Ochito “Blue” contact assembly are defined as in Figure 1 for cable assembly termination guideline and for the comparable interconnection with the USB connectors. Pins 1, 2 and pins 5, 6 were assigned as SuperSpeed pairs for high data-rate transmission. Pins 3, 4 and pins 7, 8 are for the power and the slow-speed data respectively.

Pin Contacts (P/N: 858-029-02) **Socket Contacts (P/N: 858-028-02)**

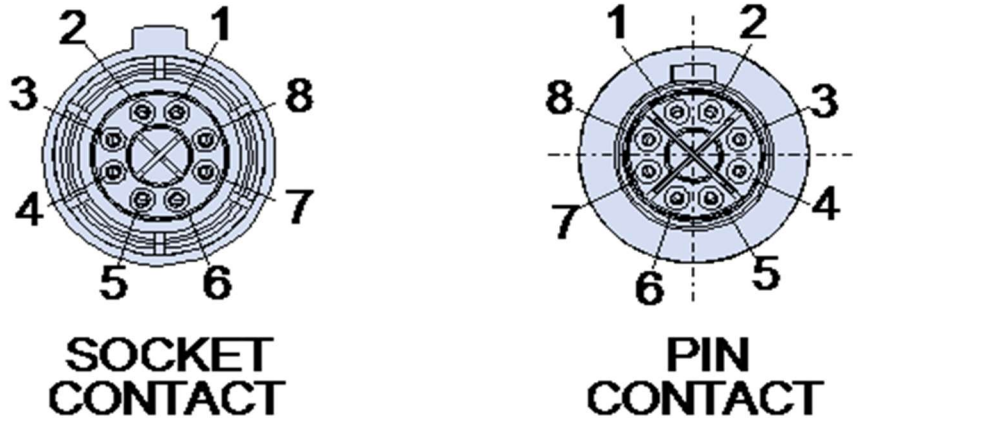


Figure 1: Ochito “Blue” Pin and Socket Pin-out Assignments

Cable Assembly Wire Diagram and Test Configurations

The cable assembly test samples were constructed using an Ochito pin contact assembly (P/N: 858-028-02) connecting to an Ochito socket contact assembly (P/N: 858-029-02) at the opposite end through USB 3.0 bulk cable (P/N: 963-110). The cable assembly was wired in 1-1 configuration manner as shown in Figure 2 or in Appendix B; the cable pairs were terminated to the same pin position of Ochito “Blue” contacts. Pins 1, 2 and pins 5, 6 were assigned as SuperSpeed signal pairs. Pins 3, 4 and pins 7, 8 are for the power and the slow-speed data respectively.

Socket Side (P1)		Bulk Cable	Pin Side (P2)	
1	Blue	◄——————►	Blue	1
2	Yellow	◄——————►	Yellow	2
3	Red	◄——————►	Red	3
4	Black	◄——————►	Black	4
5	Orange	◄——————►	Orange	5
6	Violet	◄——————►	Violet	6
7	Green	◄——————►	Green	7
8	White	◄——————►	White	8
Shell		**Cable Braid and GND_Drain**	**Shell**	

Figure 2: Ochito "Blue" Cable Assembly Wiring Diagram

Test Equipment

- Keysight E5071C 4-port Vector Network Analyzer with Optional TDR option (ENA)
- Keysight ECAL Module N4433A
- Tektronix 8300 TDR Scope with 80E08 Test Modules
- PCB test fixture assly. (P/N: 691-CB086) with mounted Ochito PCB pin contact (P/N: 82H-85179)
- PCB test fixture assly. (P/N: 691-CB086) with mounted Ochito PCB socket contact (P/N: 83H-85178)
- PCB test fixture assly. (P/N: 691-CB086) with mounted Ochito PCB Right Angle Pin contact (P/N: 792-009-10)

Test Setup and Calibration

The ENA was setup to characterize the differential s-parameters and impedance of the mated Ochito contact and cable assemblies. The setup inputs for the ENA are specified as below:

Frequency Sweep:	10 MHz – 20 GHz
IF Bandwidth:	500 Hz
Resolution:	2001 Points
Power Level:	-5.0dBm

A full 4-port calibration was performed using the ECAL module as illustrated in Figure 3 before commencing test of the mated contact and the cable assemblies.

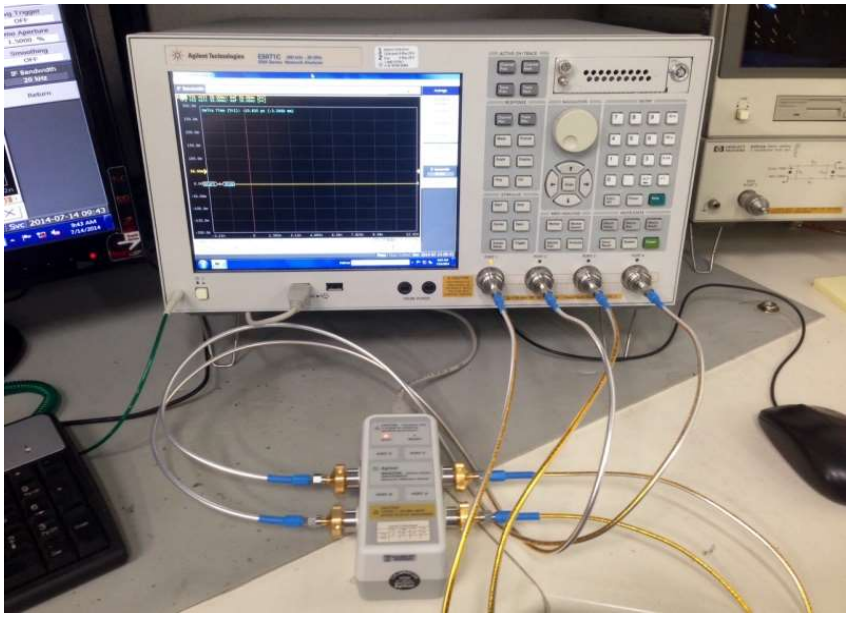


Figure 3: ENA Test Setup and Calibration

Test Procedure

1. PCB Test Fixture

The PCB test fixture for the Ochito “Blue” qualification test for USB 3.1 SI compliance is shown in the Appendix A. All part of the PCB test fixture is excluded from the test result of the contact and the cable assemblies.
The test fixture was first characterized for the impedance performance using the TDR scope to ensure a good impedance match; and then it was tested for the thru s-parameter (SDD21). The s-parameter data was saved in a touchstone (.s4p) format. The s-parameter data would later be used for de-embedding the test fixture from the mated Ochito contact and cable assembly test results.

2. Mated Ochito Contact

The mated Ochito contact assembly under SI characterization test is considered from back-end of the socket contact to the back-end of the mated pin contact as shown in Figure 4.
For SI performance test, the Ochito contacts were mounted on the PCB test fixture assembly (P/N: 961-CB086). The pin and socket contacts then mated together as shown in Figure 4. During test, all un-active ports on the test boards that are not under test were terminated with 50-Ohm loads.

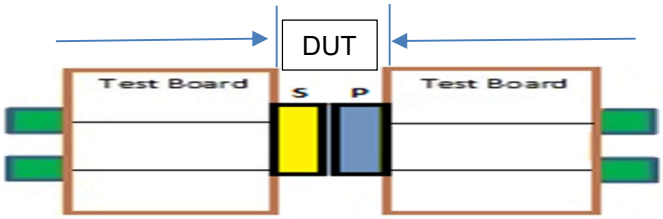


Figure 4: Ochito “Blue” Mated Pin and Socket for Test

Using the ENA and/or TDR scope to collect the defined frequency domain and time domain test parameters in the USB 3.1 standard below.

- Impedance (of SuperSpeed pairs) @ 50ps signal rise time using the TDR scope
- SDD21 (of SuperSpeed pairs)
- SDD11/SDD22 (of SuperSpeed pairs)
- SCD21 (of SuperSpeed pairs)
- Near-end crosstalk or NEXT (between SuperSpeed Pairs)
- NEXT (between SuperSpeed pair and D+/D- pair)
- Far-end crosstalk or FEXT (between SuperSpeed pair and D+/D- pair)

The test data was saved in a touchstone (.s4p) format for the s-parameters and in a .csv format for the impedance data. All part of the PCB test fixture artifact that is not part of the mated contact would be de-embedded out by using the Ataitec software and the s-parameter data of the PCB test fixture.

3. Ochito Cable Assembly

The Ochito cable assembly under test is considered from the first mated pin/socket to the last mated pin/socket as shown in Figure 5 & 6.
For the SI performance test, two cable assembly configurations and lengths were evaluated. One configuration under test included a total of 2 mated Ochito contact connections (A + B) in the cable assembly as shown in Figure 5. The other optional configuration included a total of 3 connections (A+B+C) as shown in Figure 6.
During test all un-active ports on the test boards that are not under test were terminated with 50-Ohm loads.
Using the ENA and/or TDR scope to collect the defined frequency domain and time domain test parameters in the USB 3.1 standard below.

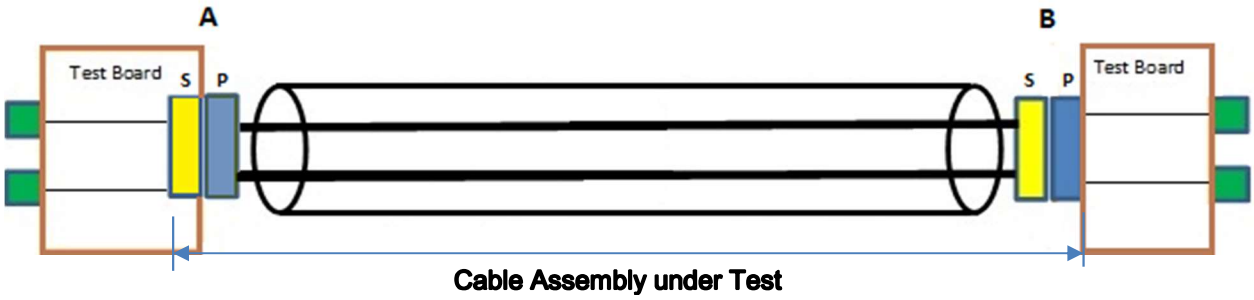


Figure 5: Test Configuration for each 0.3m and 1.5m Length Cable Assembly Test

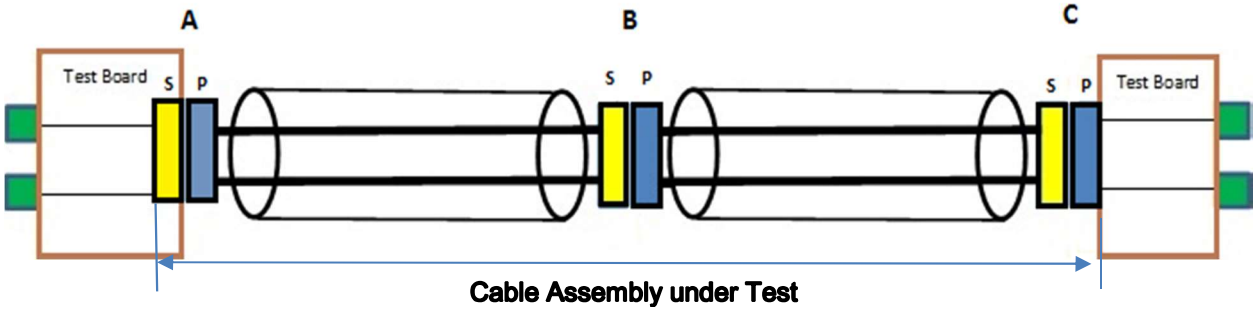


Figure 6: Test Configuration for Interconnected 0.3m and 1.5m (1.8m Total) Length Cable Assembly Test

- Impedance (of SuperSpeed pairs) @ 50ps signal rise time using the TDR scope; include part of the bulk cable and mated contact for the test
- SDD21 (of SuperSpeed pairs)
- SDD11/SDD22 (of SuperSpeed pairs)
- SCD21 (of SuperSpeed pairs)
- Near-end crosstalk or NEXT (between SuperSpeed Pairs)
- NEXT (between SuperSpeed pair and D+/D- pair)
- Far-end crosstalk or FEXT (between SuperSpeed pair and D+/D- pair)

The test data was saved in a touchstone (.s4p) format for the s-parameters and in a .csv format for the impedance data. All part of the PCB test fixture artifact that is not part of the cable assemblies would be de-embedded out by using the Ataitec software and the s-parameter data of the PCB test fixture.

Test Results

The following data represents a typical signal integrity performance of the Ochito “Blue” mated crimp contact and cable assemblies made from the USB 3.1 bulk cable part number specified in this document.

1. Mated Contact SI Performance

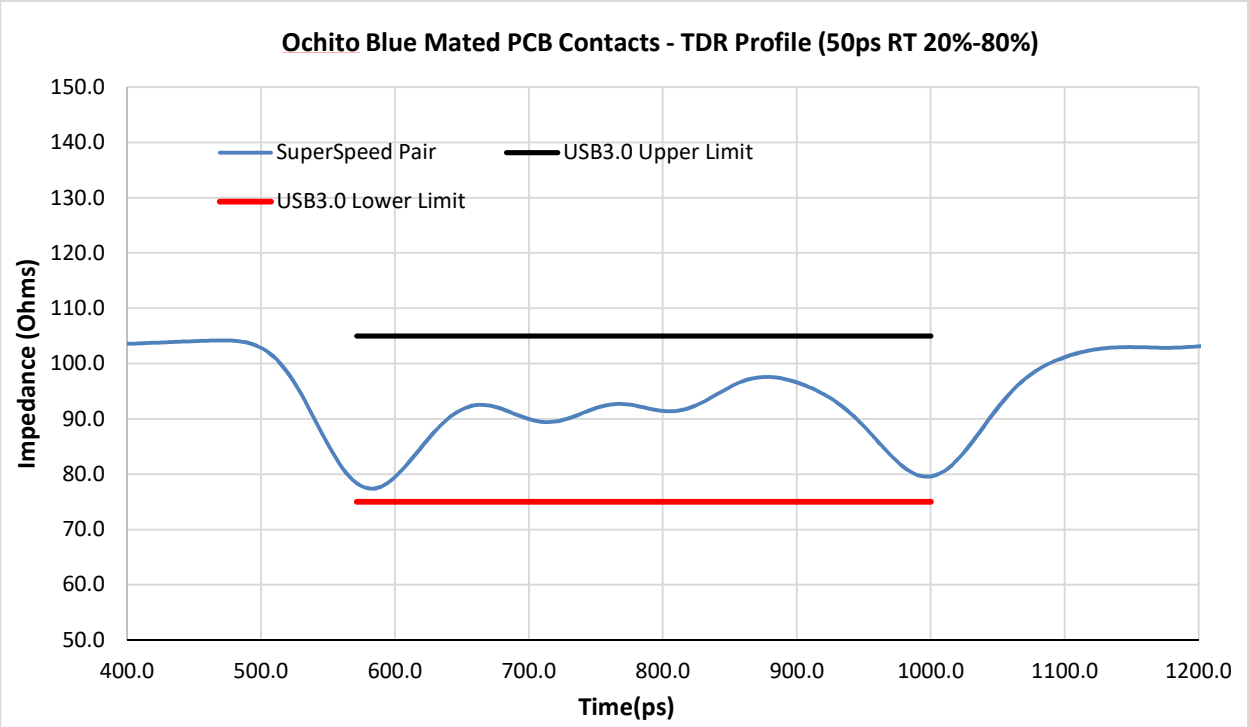


Figure 7: Mated Ochito Contact - Diff. TDR Profile @50ps Signal Rise time

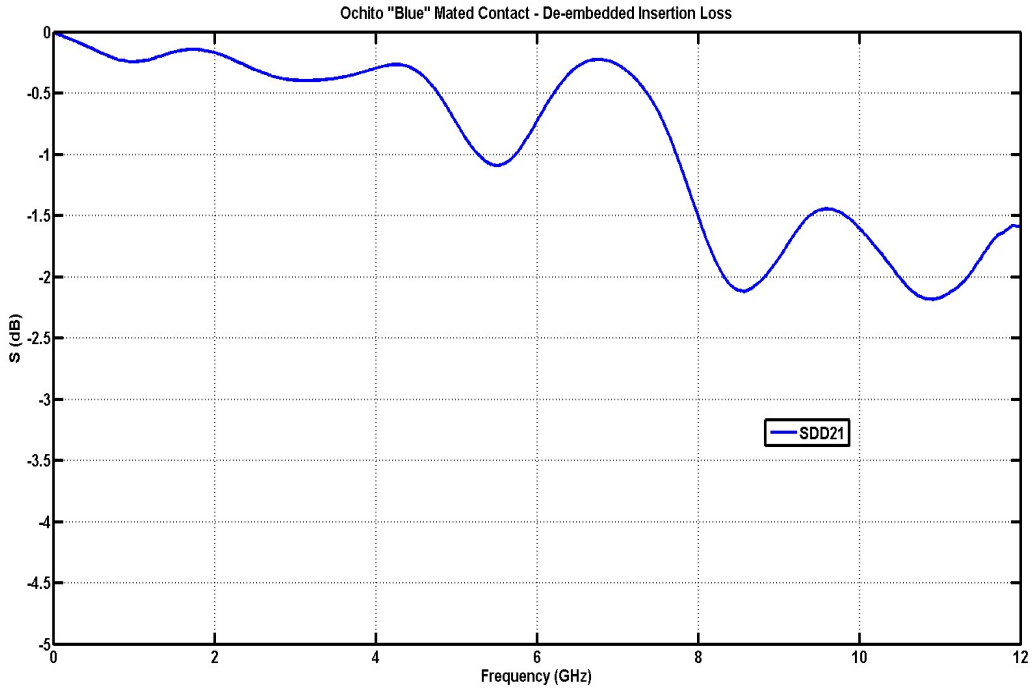


Figure 8: Mated Ochito Contact - De-embedded Insertion Loss (SDD21)

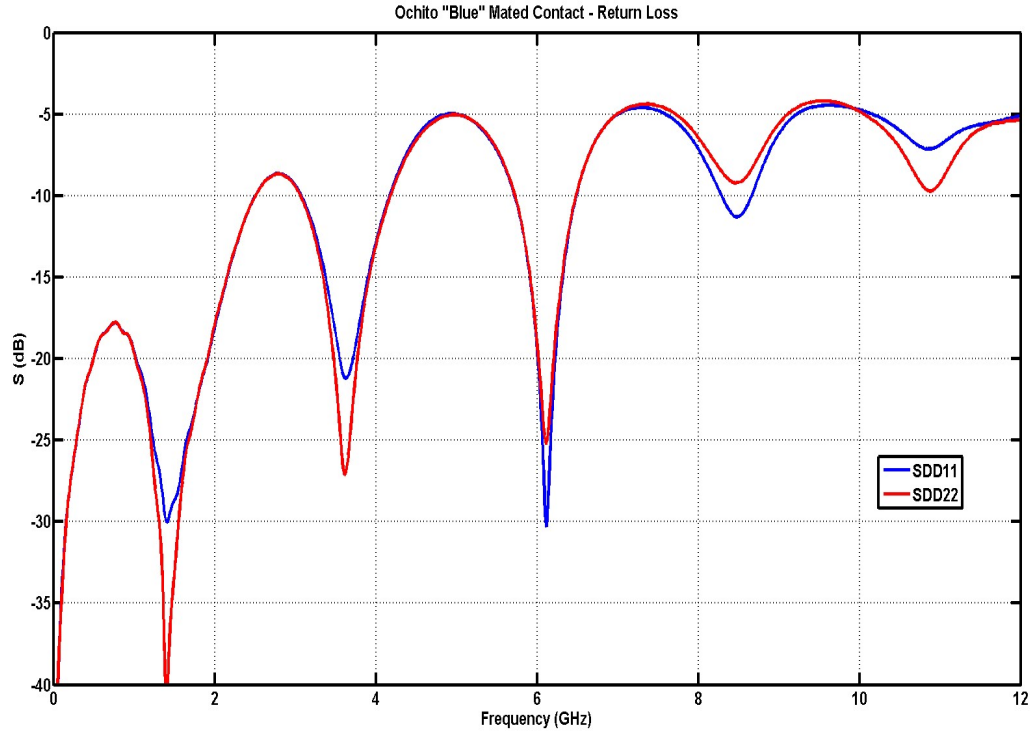


Figure 9: Mated Ochito Contact - Return Loss (SDD11/SDD22)

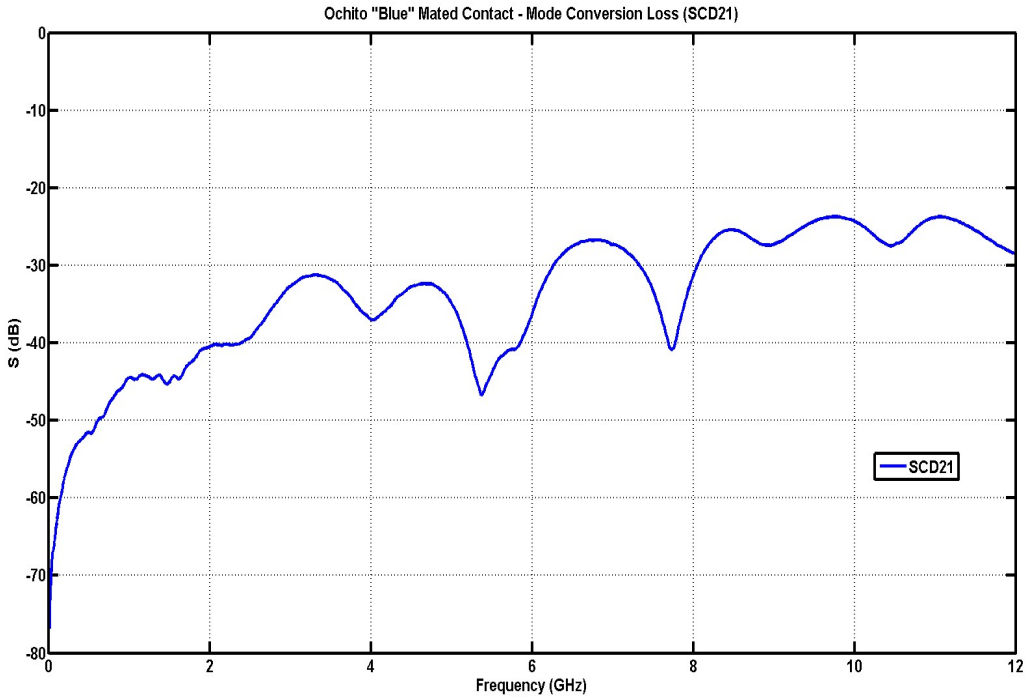


Figure 10: Mated Ochito Contact – Mode Conversion Loss (SCD21)

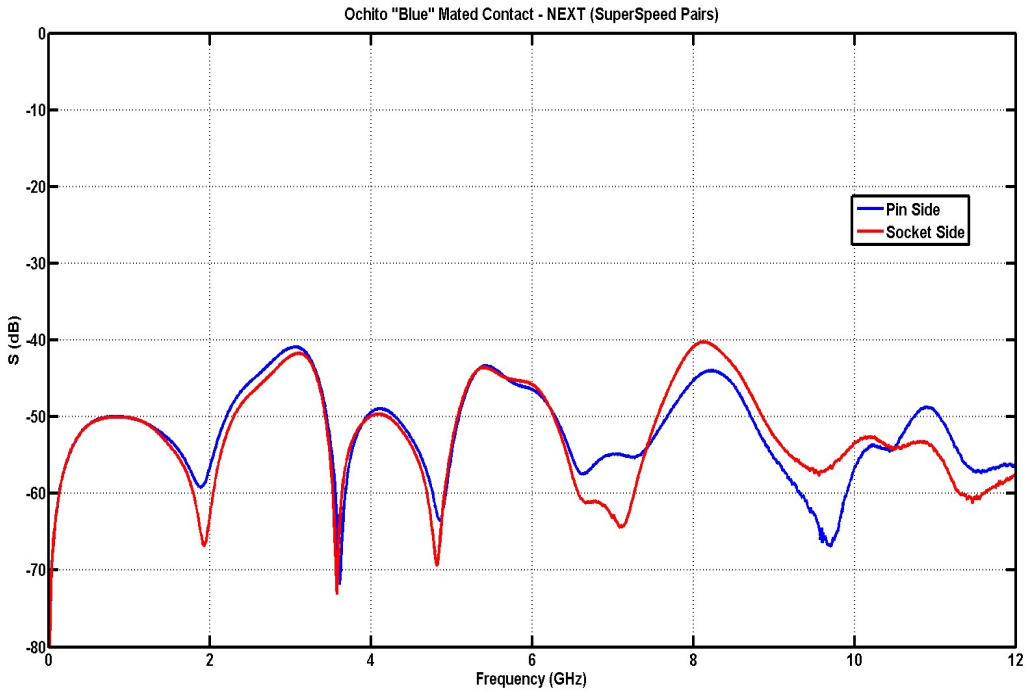


Figure 11: Mated Ochito Contact – NEXT (SuperSpeed Pairs)

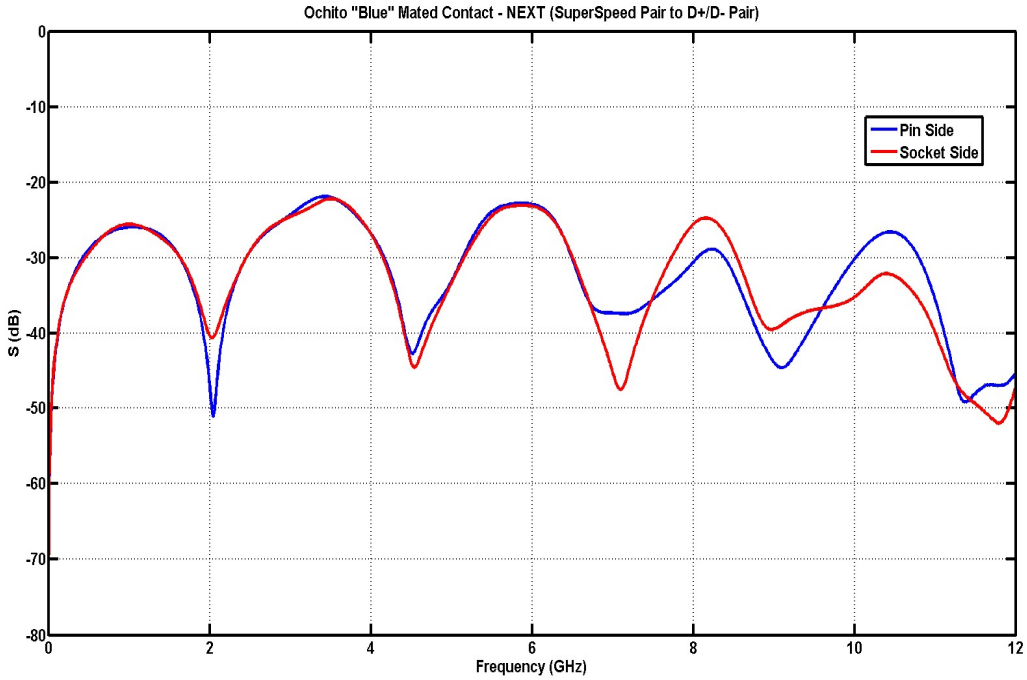


Figure 12: Mated Ochito Contact – NEXT (SuperSpeed pair to D+/D- pair)

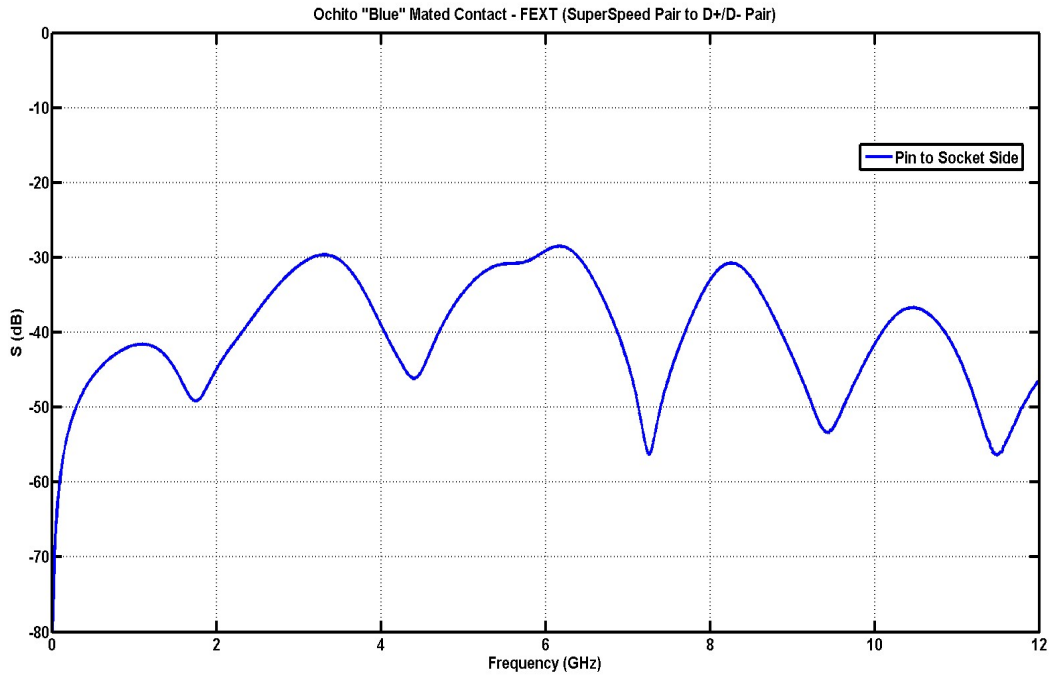


Figure 13: Mated Ochito Contact – FEXT (SuperSpeed pair to D+/D- pair)

2. Cable Assembly SI Performance

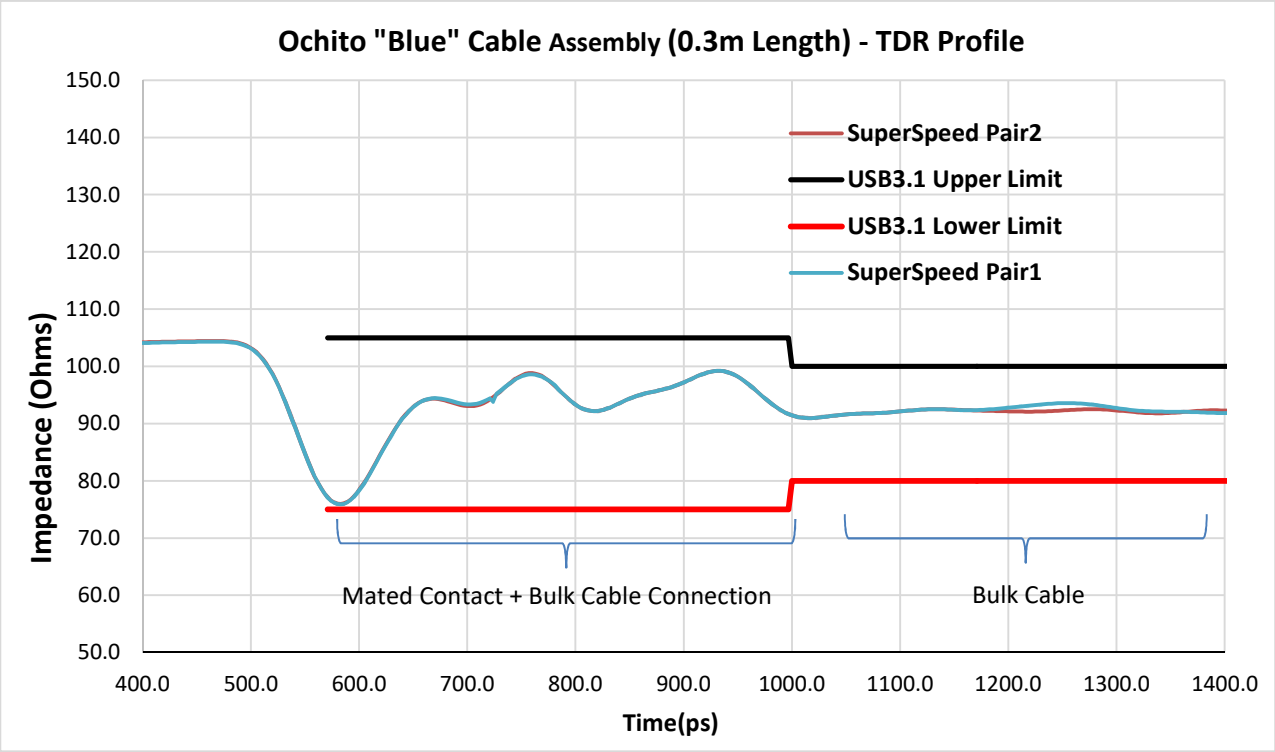


Figure 14: 0.3m Cable Assembly – Diff. TDR of Contact/Cable Connection @50ps Signal Rise Time

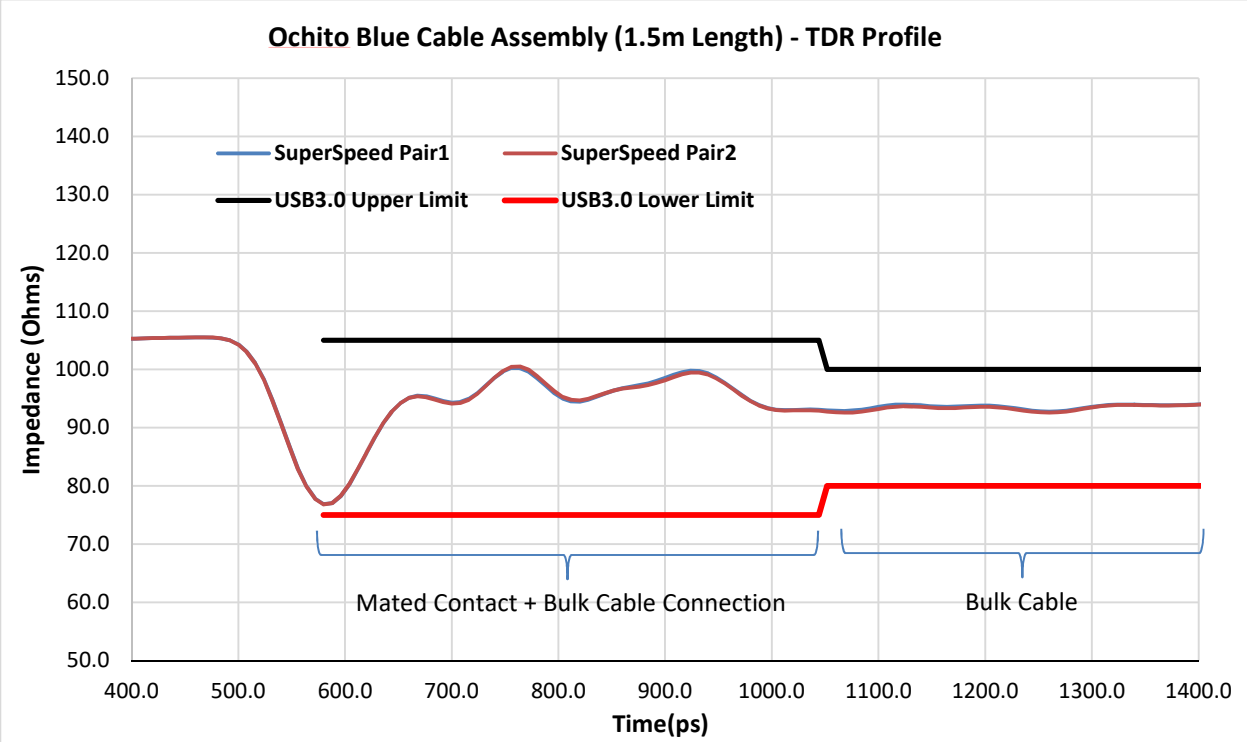


Figure 15: 1.5m Cable Assembly – Diff. TDR of Contact/Cable Connection @50ps Signal Rise Time

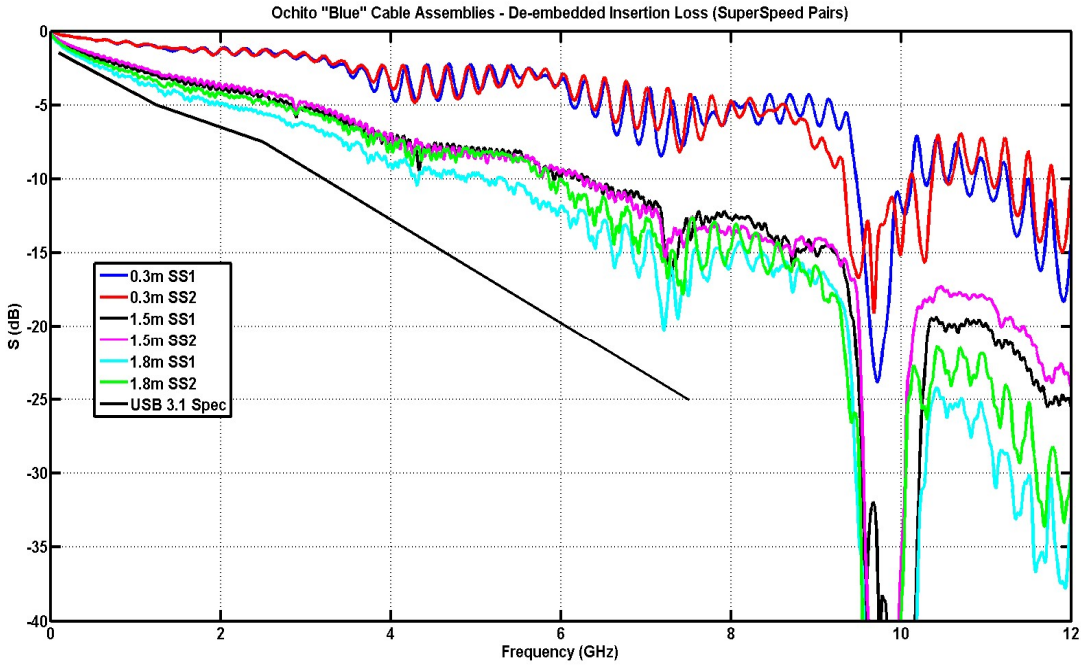


Figure 16: Cable Assemblies - De-embedded Insert Loss (SDD21)

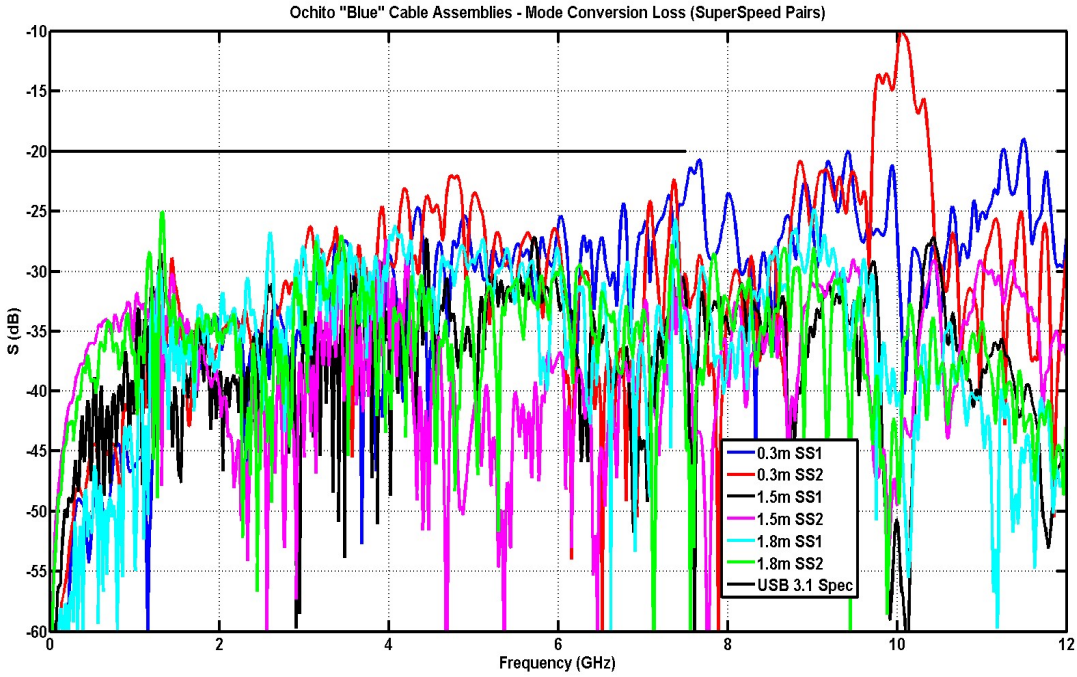


Figure 17: Cable Assemblies - Mode Conversion Loss (SCD21)

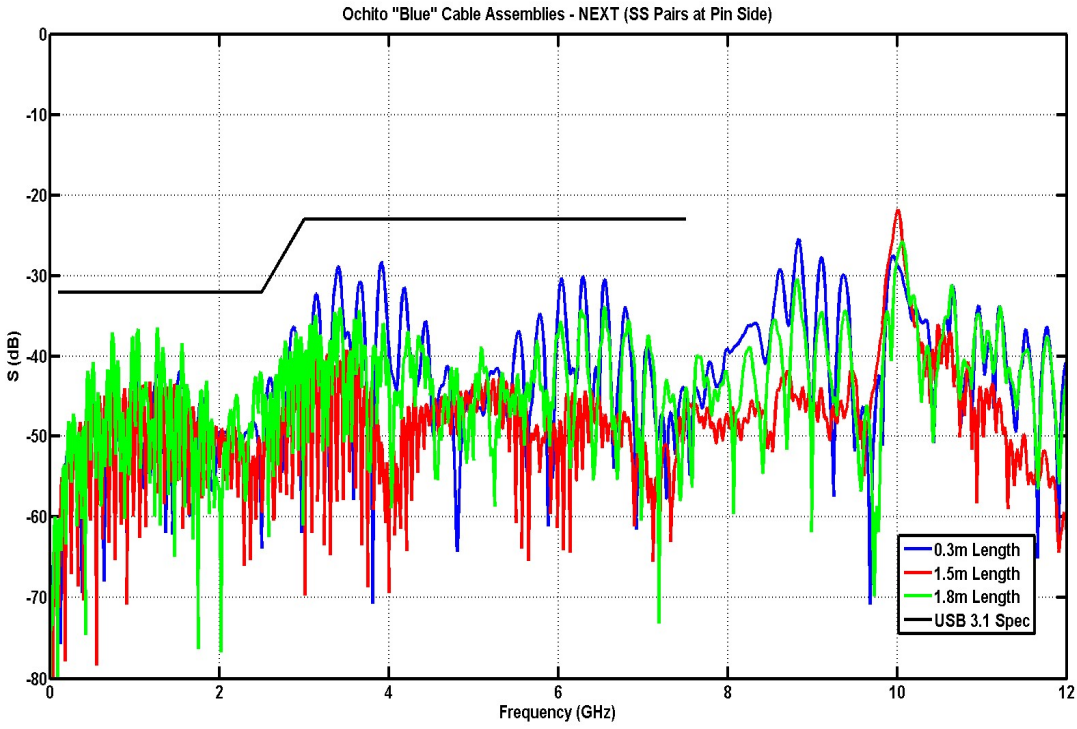


Figure 18: Cable Assemblies - NEXT (SuperSpeed Pairs)

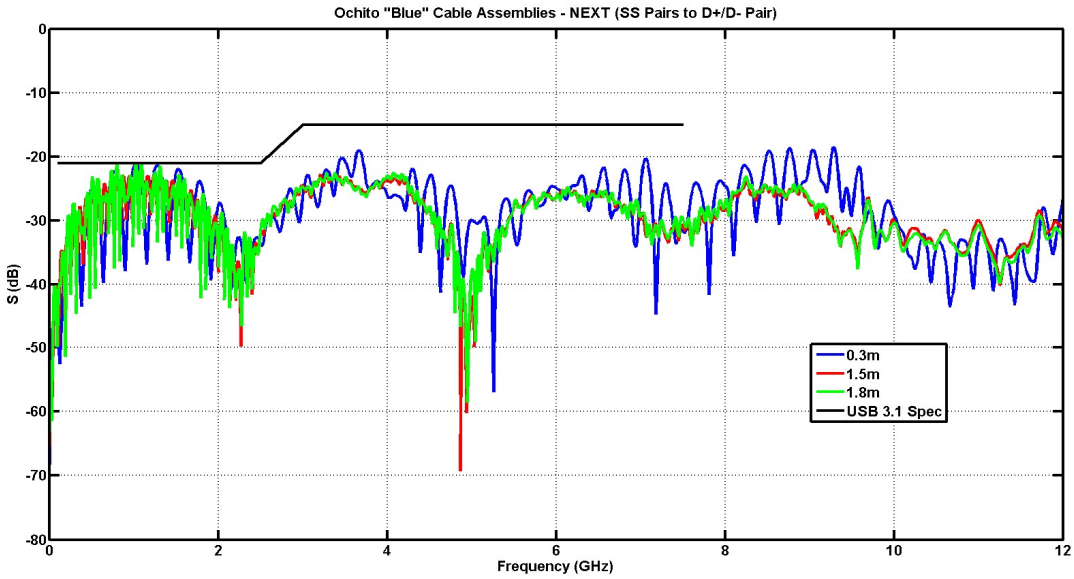


Figure 19: Cable Assemblies – NEXT (SuperSpeed Pair to D+/D- Pair)

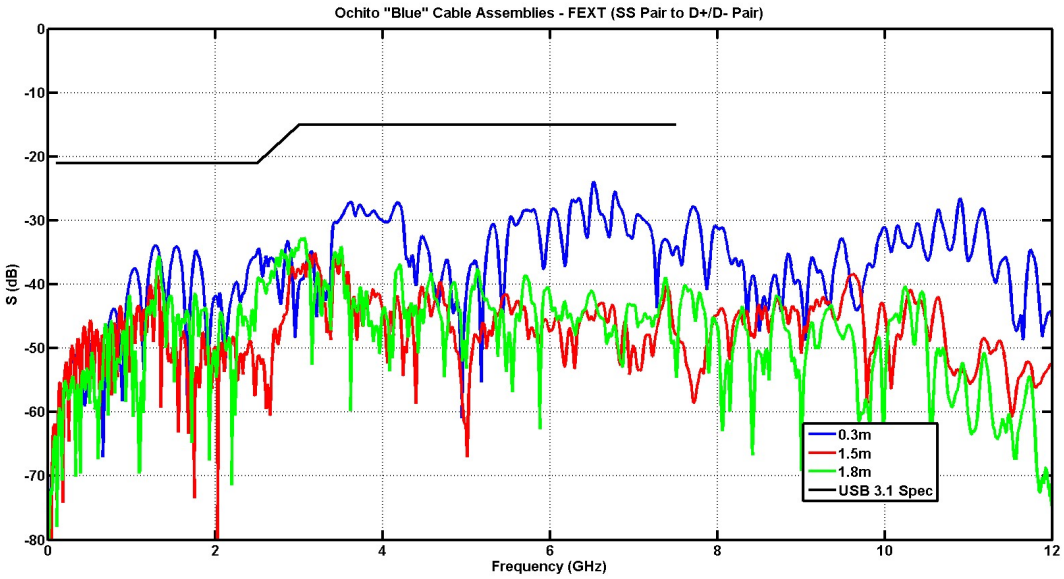


Figure 20: Cable Assemblies - FEXT (SuperSpeed Pair to D+/D- Pair)

Conclusion

Based on the test results obtained, Glenair Ochito “Blue” cable assemblies in high confidence can provide an adequate bandwidth to support the USB 3.1 Gen 1 data transmission application as defined in the standard. The maximum cable assembly length will be determined by the bulk cable performance and the total number of cable assembly connections between the host equipment and the devices.

Appendix A – Ochito “Blue” Test Fixture and SI Characteristics

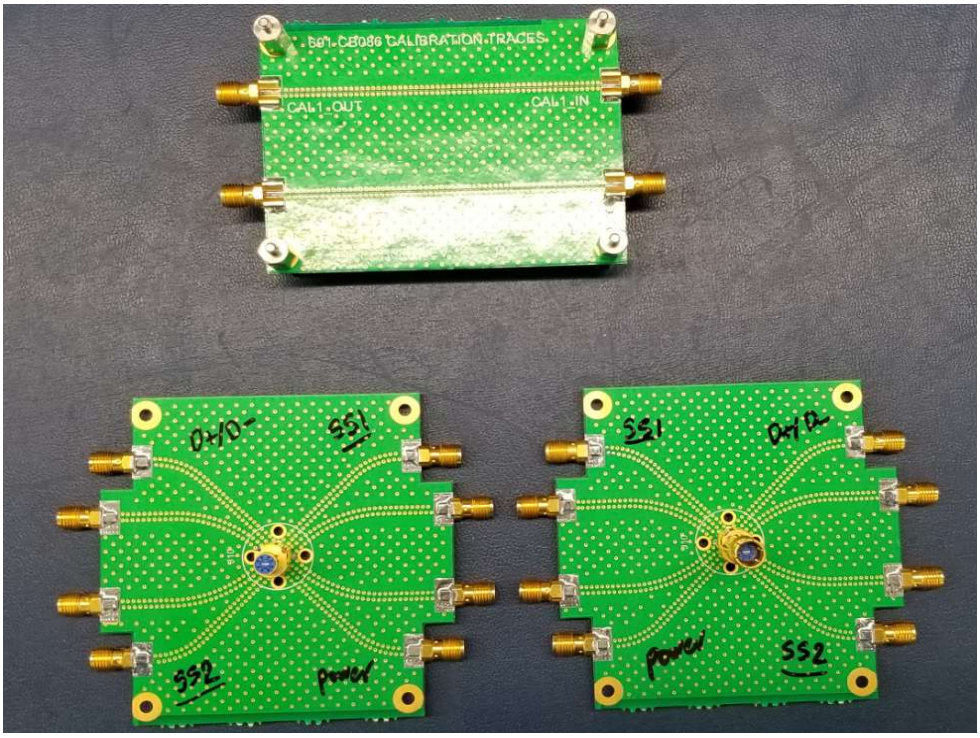


Figure 21: Ochito “Blue” Test Boards and Calibration Artifacts

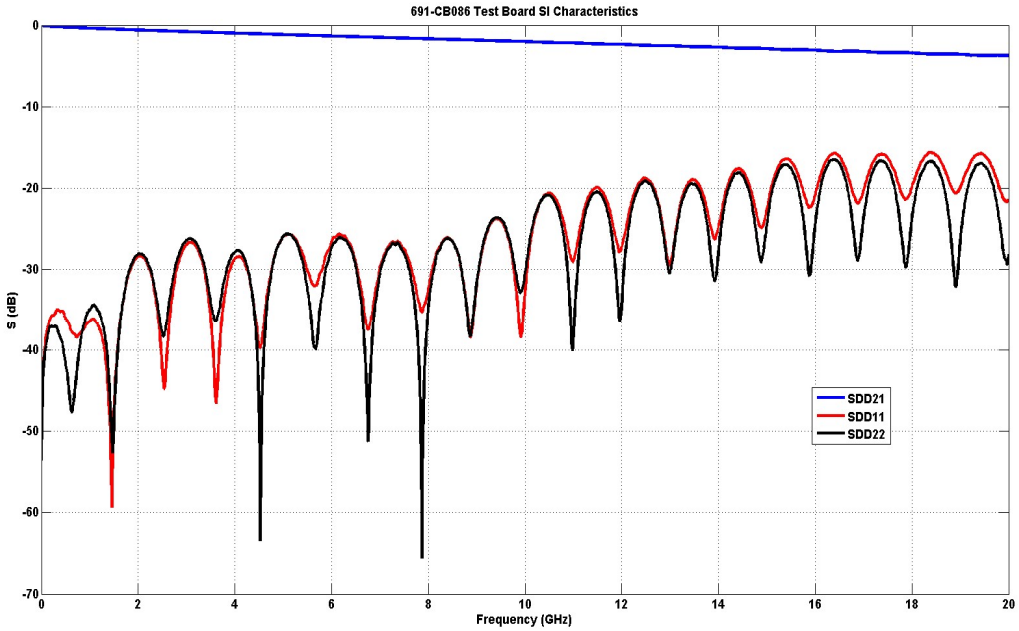
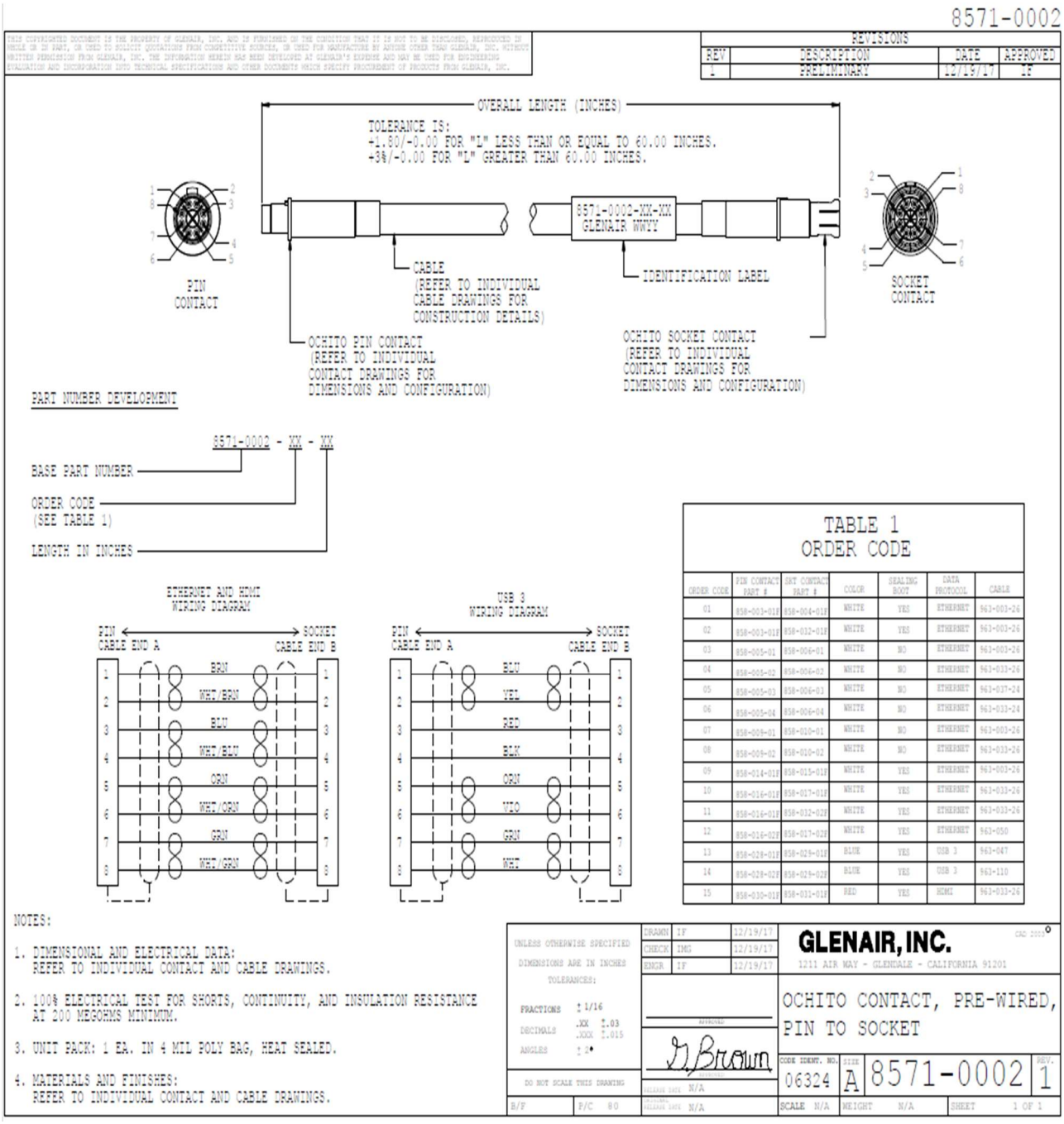


Figure 22: 2X Calibration PCB Trace Characteristics

Appendix B – Ochito “Blue” Cable Assembly Drawing



Appendix C – Ochito “Blue” PCB-Mount Right Angle Contact SI Performance

The following results include the SI test data of a mated right angle Ochito “Blue” contact.

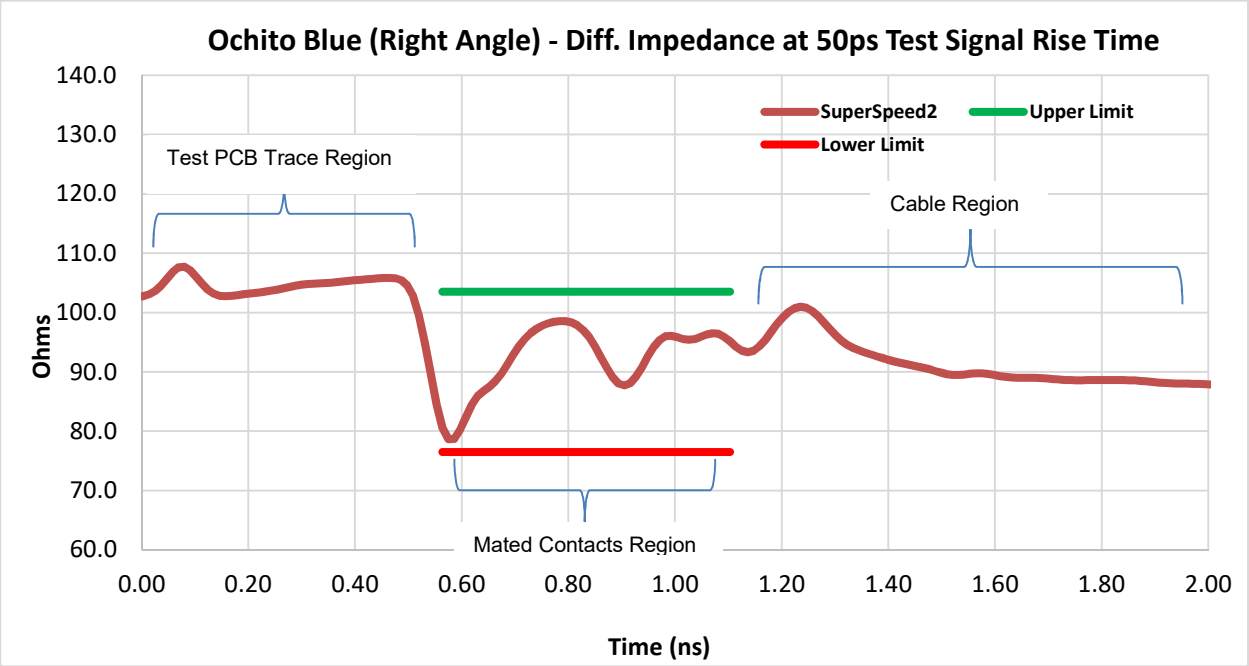


Figure 23: Ochito "Blue" Right Angle Contact (Mated) – Diff. Impedance

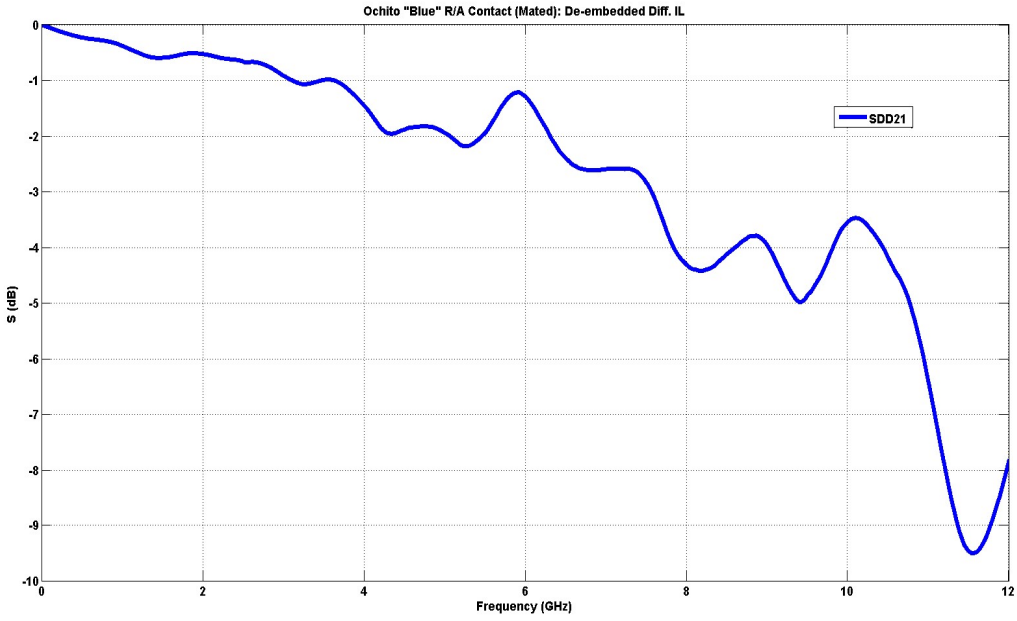


Figure 24: Ochito "Blue" Right Angle Contact (Mated) - De-embedded Insertion Loss

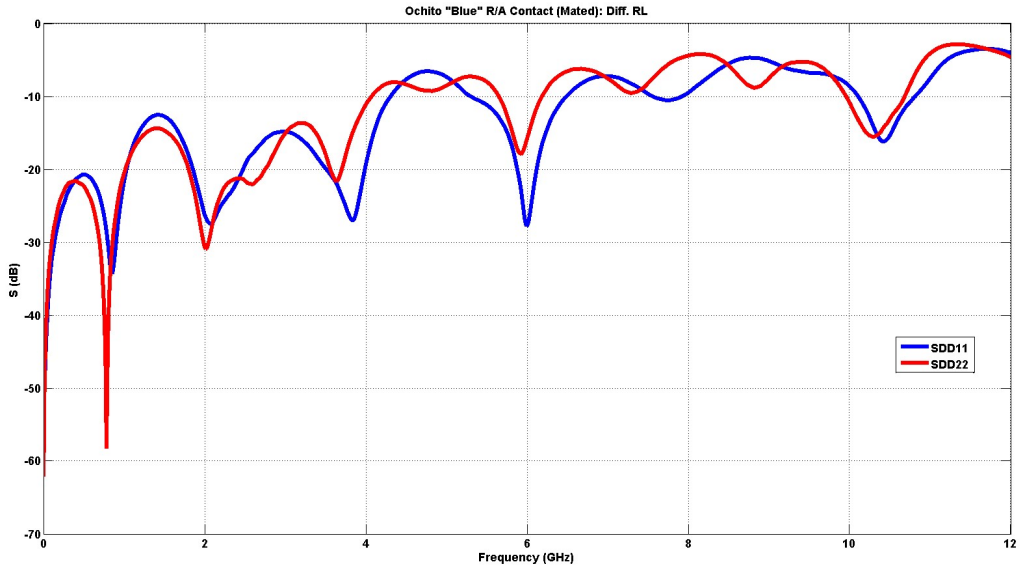


Figure 25: Ochito "Blue" Right Angle Contact (Mated) - Diff. RL

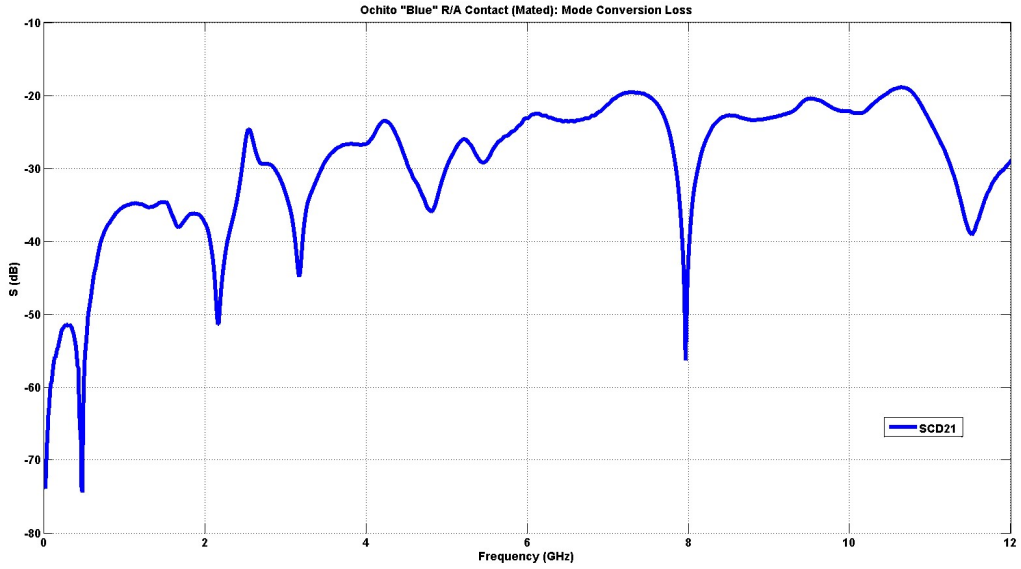


Figure 26: Ochito "Blue" Right Angle (Mated) - Mode Conversion Loss

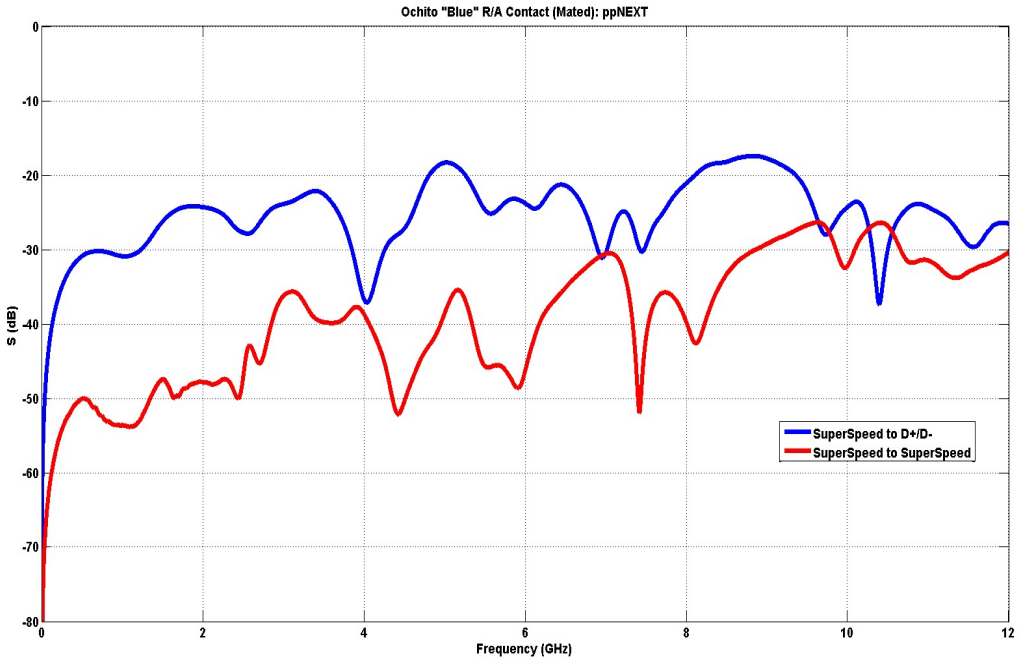


Figure 27: Ochito "Blue" Right Angle (Mated) – Pair to Pair NEXT

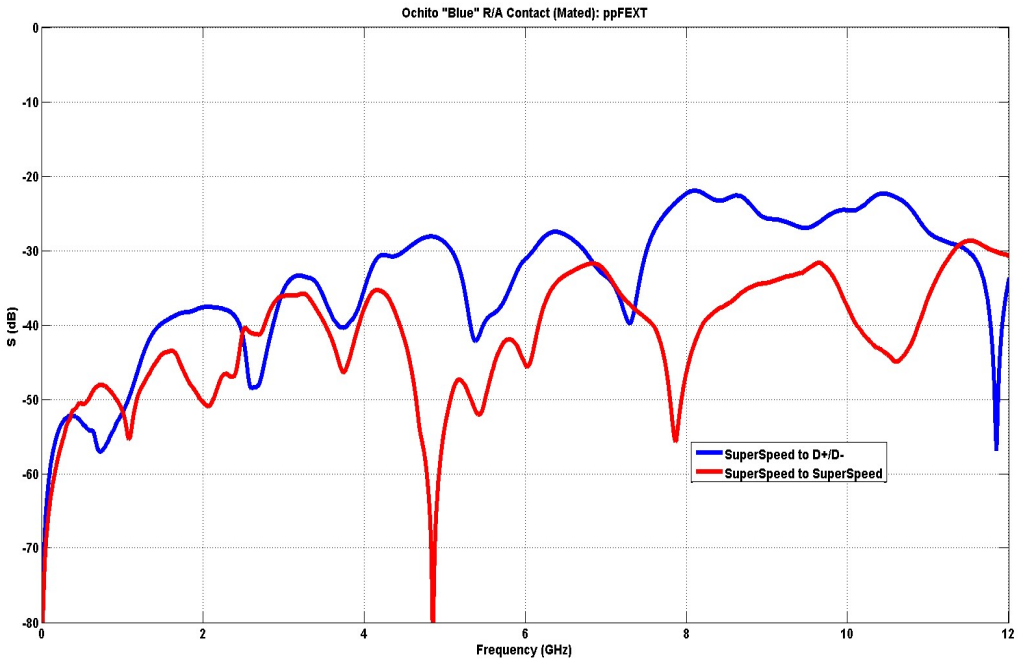


Figure 28: Ochito "Blue" Right Angle (Mated) - Pair to Pair FEXT